ABSTRACT

Methods and apparatus are disclosed for providing multiple clock signals on a chip using a second phase-locked loop library circuit connected to a buffered reference clock output of a first PLL library circuit which may be used, *inter alia*, in a computer or communications system, such as a computer or communications device, packet switching system, router, other device, or component thereof. Known prior circuits would typically use multiple off-chip reference clock signals for those applications that require multiple reference clocks. Implementations according to the invention may be particularly useful for possibly providing a lower-cost solution when, for example, such a circuit provides the capability to maintain tight timing, without sacrificing input pins, or excessively loading the PC board's clock driver. Various implementations of such circuits include an ASIC or those using any chip implementation technology or combinations of technologies, including but not limited to VLSI design and discrete components.